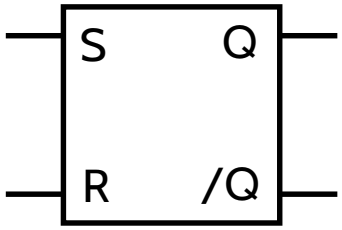
POLYTECH ANGERS

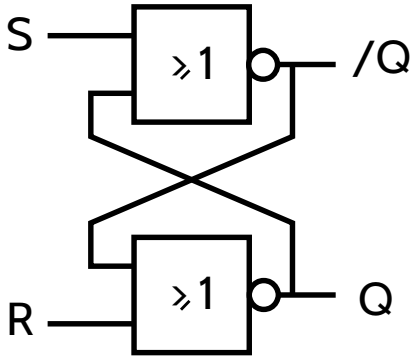
Électronique Numérique

Les bascules

Rémy Guyonneau
Sylvain Pezeril

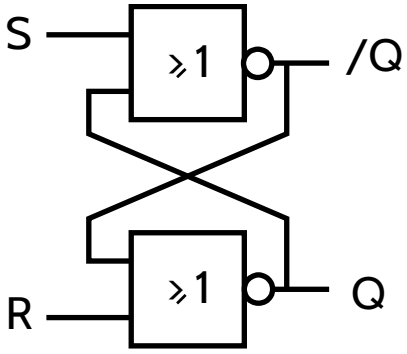
Le bistable RS





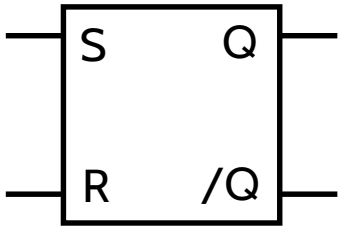
S : Set, entrée de mise à 1
R : Reset, entrée de mise à 0

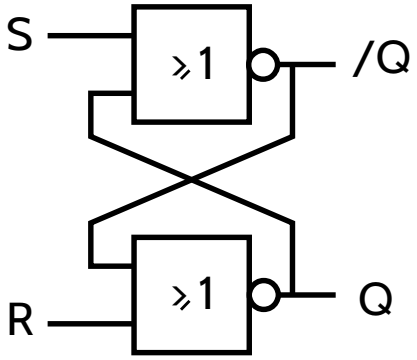
- Analyse



S	R	Q
0	0	
0	1	
1	0	
1	1	

Le bistable RS





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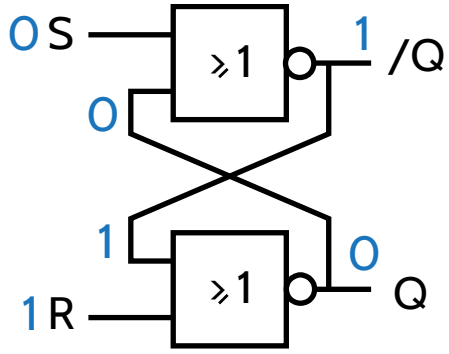
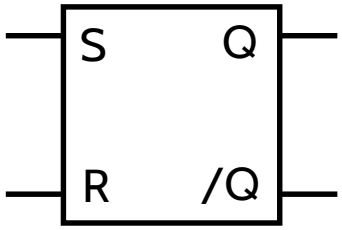
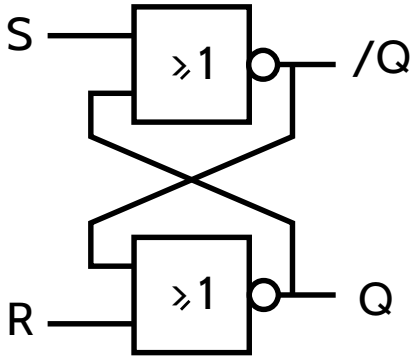


$\overline{1 + x} = 0$

S	R	Q
0	0	
0	1	0
1	0	
1	1	

Le bistable RS





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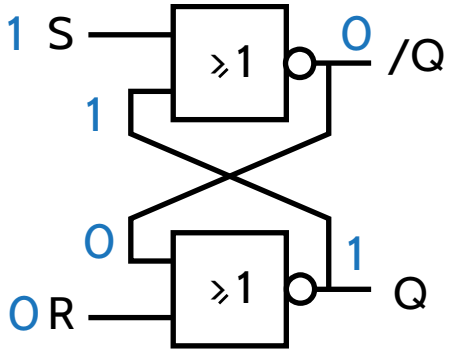
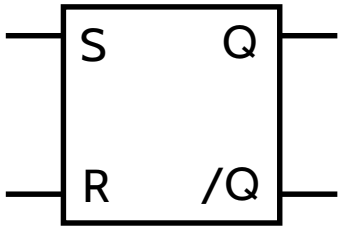
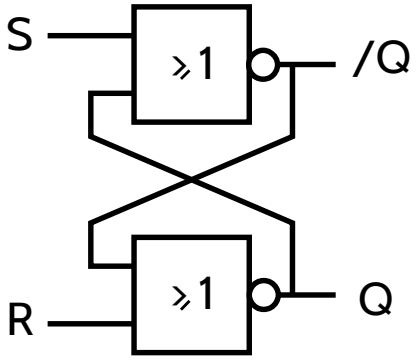


$\overline{1 + x} = 0$

S	R	Q
0	0	
0	1	0
1	0	1
1	1	

Le bistable RS





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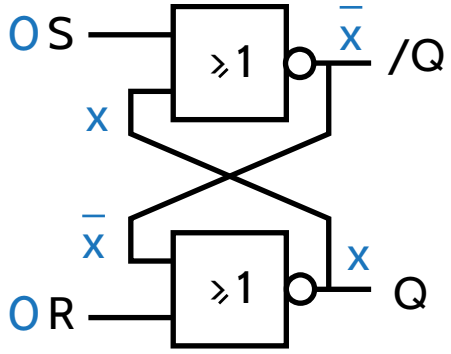
R : Reset, entrée de mise à 0

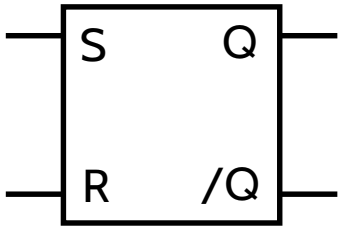
- Analyse

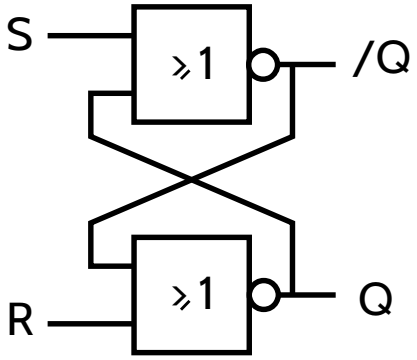


$\overline{0 + x} = \overline{x}$

S	R	Q
0	0	inchangée
0	1	0
1	0	1
1	1	

Le bistable RS





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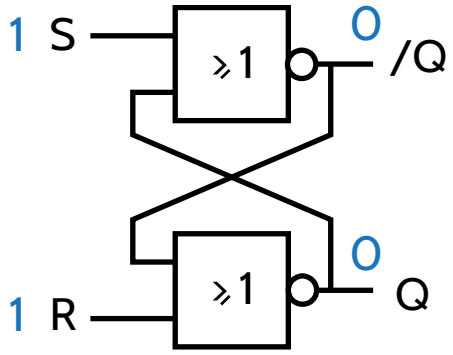
R : Reset, entrée de mise à 0

- Analyse



$\overline{1 + x} = 0$

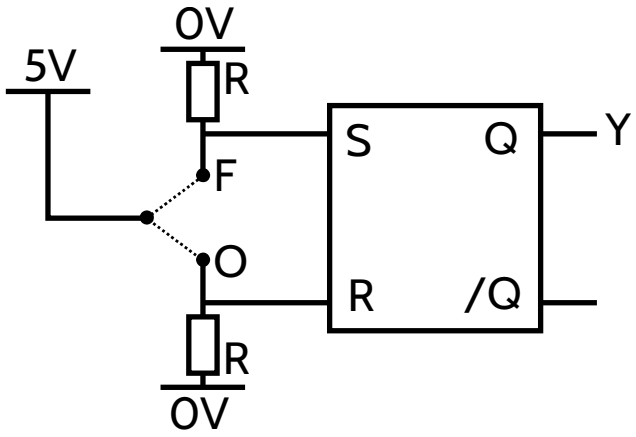
S	R	Q
0	0	inchangée
0	1	0
1	0	1
1	1	interdit

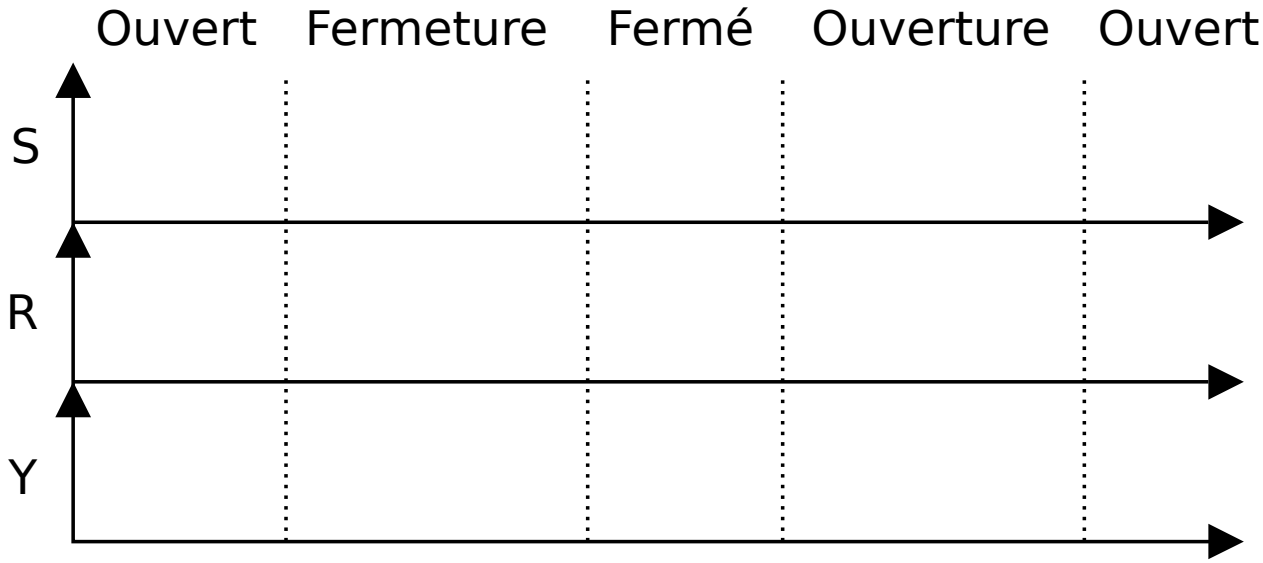
Le bistable RS

- On constate que pour un état des entrées (S=R=0), il existe deux états de sortie possible : Q=0 ou Q=1
- On appelle système logique séquentiel tout système qui admet pour un état d'entrée plusieurs états de sorties possibles. La sortie est fonction des entrées mais aussi de ce qui s'est passé auparavant.

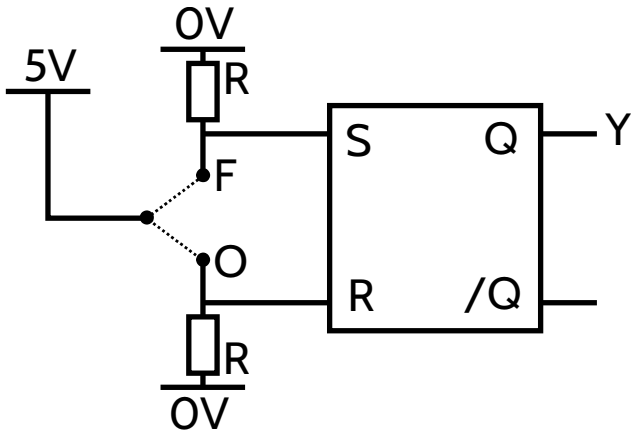
S	R	Q
0	0	inchangée
0	1	0
1	0	1
1	1	interdit

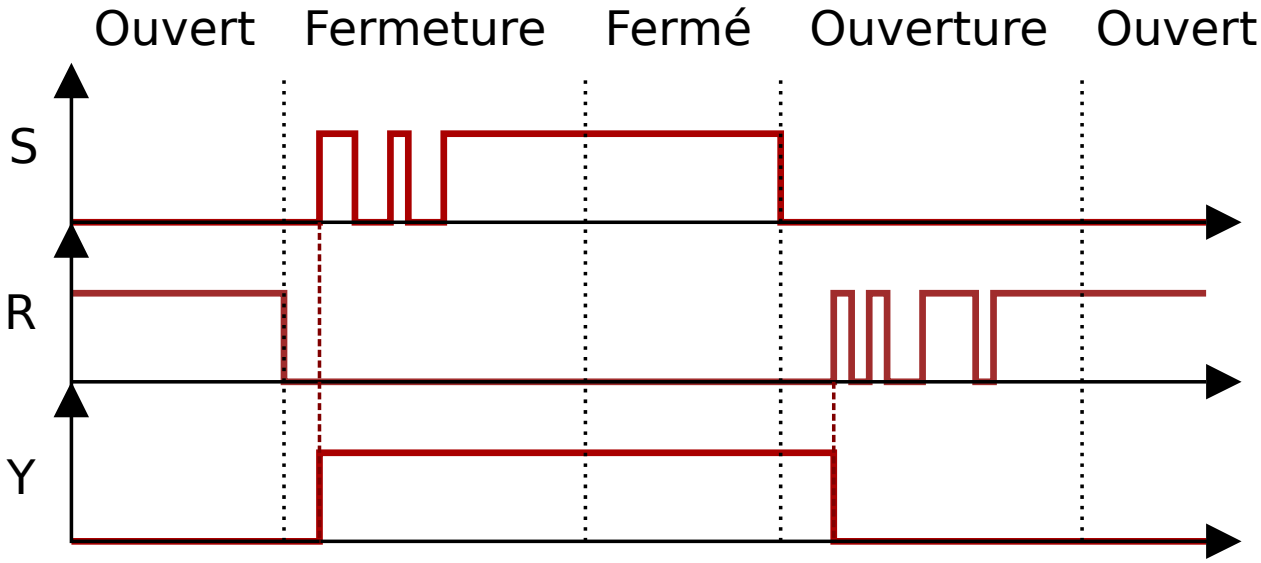
Le bistable RS - exercice



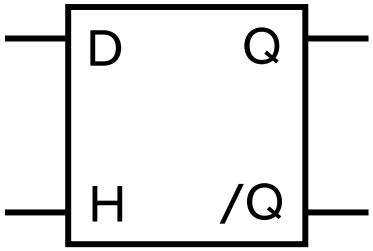


Le bistable RS - exercice

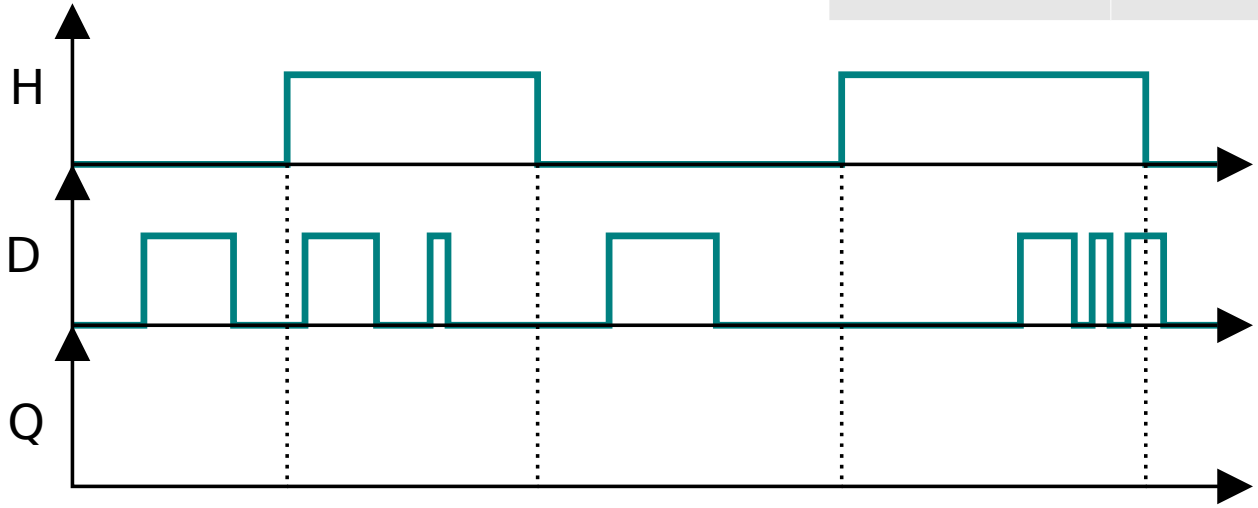




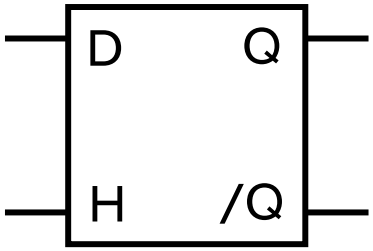
Le verrou (latch) D



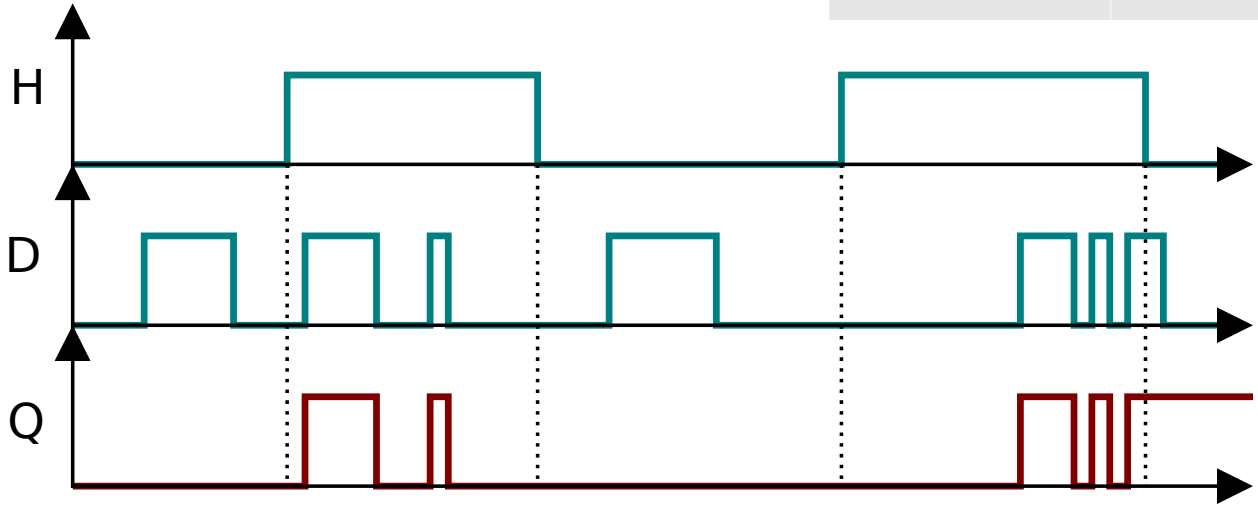
H	Q
0	Inchangée
1	D



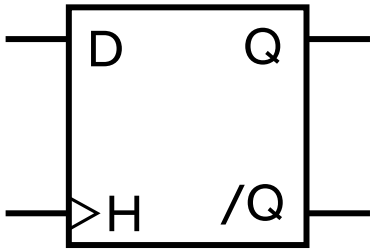
Le verrou (latch) D

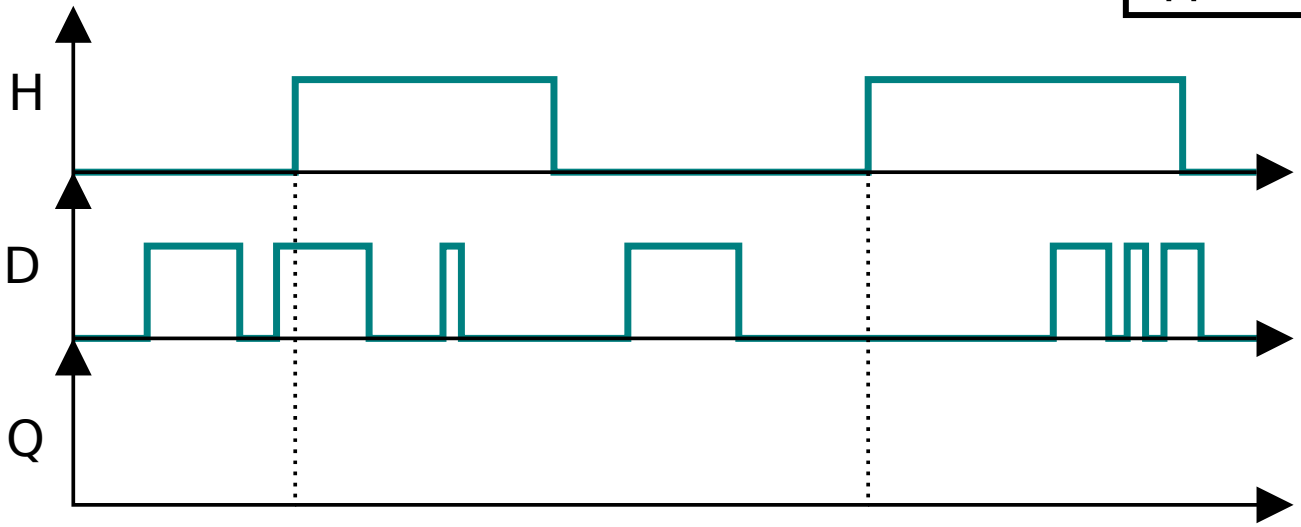


H	Q
0	Inchangée
1	D



La bascule D

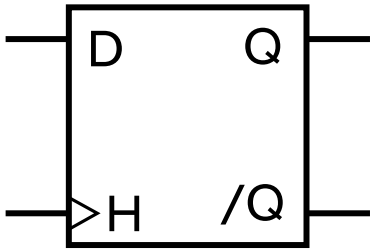




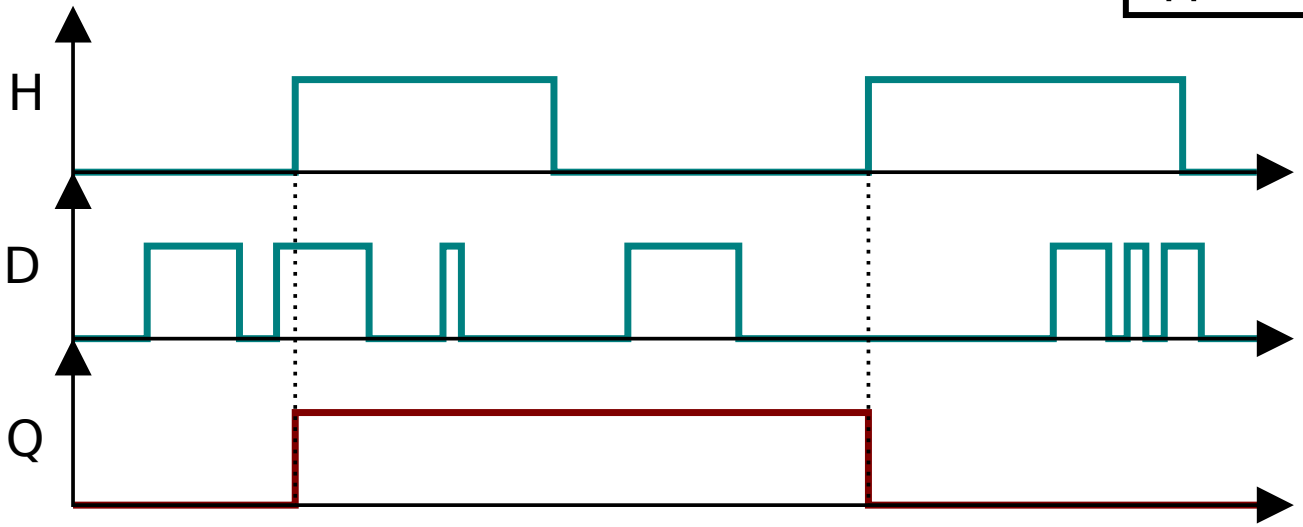
H	D_n	Q_{n+1}
0/1	X	Q_n
↑	0	0
↑	1	1

H	Q_{n+1}
0/1	Q_n
↑	D_n

La bascule D



H	D_n	Q_{n+1}
0/1	X	Q_n
↑	0	0
↑	1	1



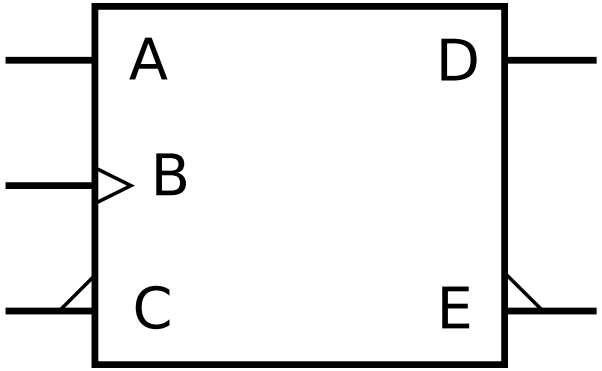
H	Q_{n+1}
0/1	Q_n
↑	D_n

La bascule D

- On constate que la sortie Q recopie l'entrée D à chaque front montant de l'horloge
- Système synchrone
  - Tout système disposant d'une entrée « horloge » qui fixe les instants des éventuels changements des sorties

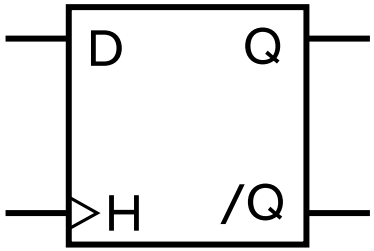
La bascule D

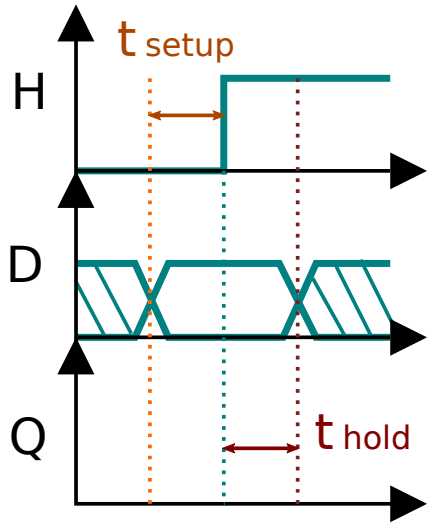
- Notations
  - A est un entrée classique
  - B est une horloge (entrée)
  - C est une entrée complémentée
  - D est une sortie classique
  - E est une sortie complémentée



La bascule D

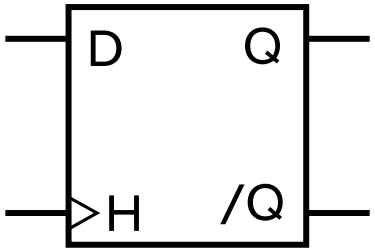
- Pour assurer le fonctionnement correct de la bascule
- t_{setup} ou t_{su} : temps de prépositionnement
  - Temps avant le front d'horloge pendant lequel la donnée doit être stable
- t_{hold} ou t_h : temps de maintien
  - Temps après le front d'horloge pendant lequel la donnée doit être stable

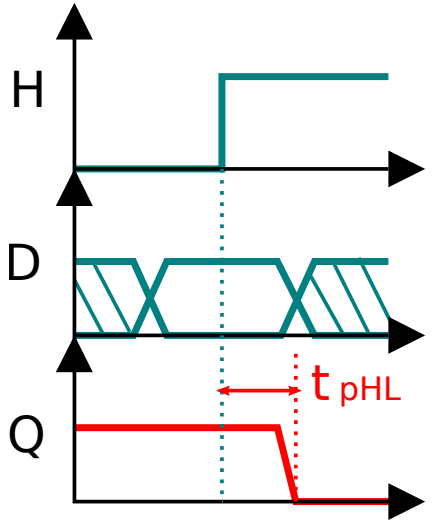




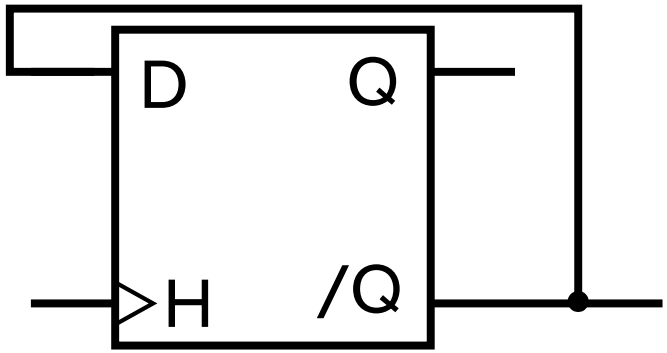
La bascule D

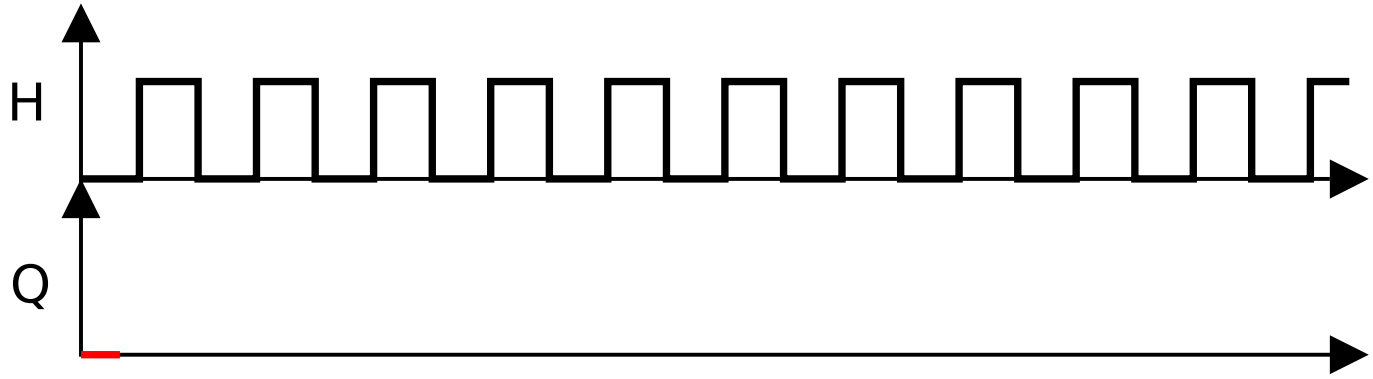
- t_p : temps de propagation
  - t_{pHL}
    - High to Low
  - t_{pLH}
    - Low to High





La bascule D – exercice 1





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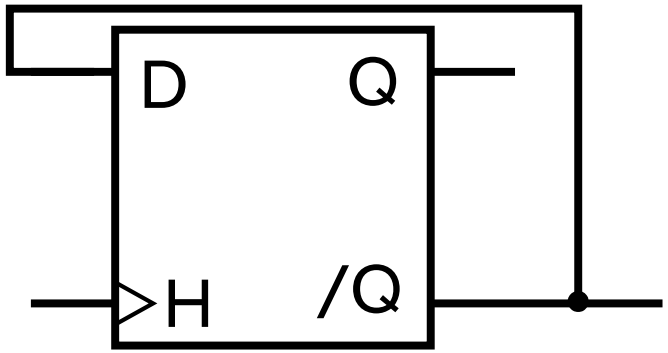
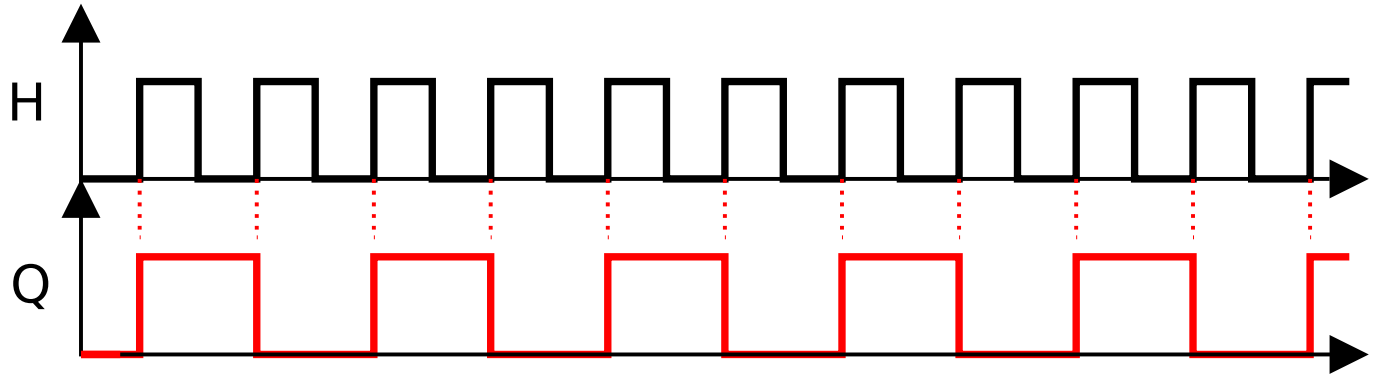
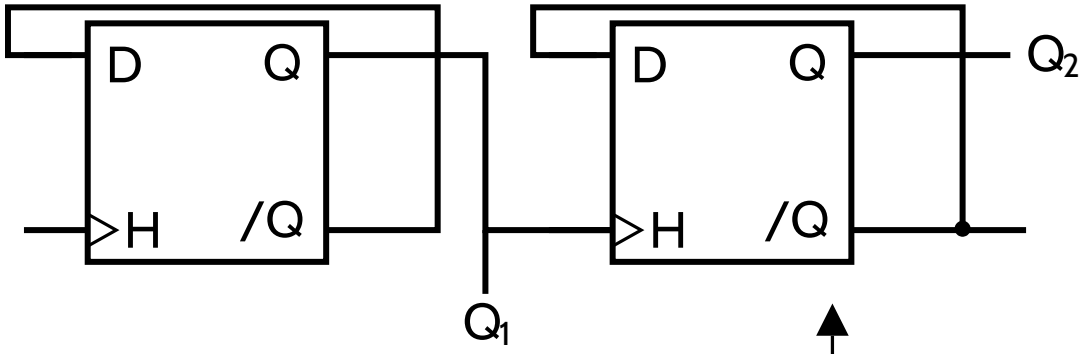
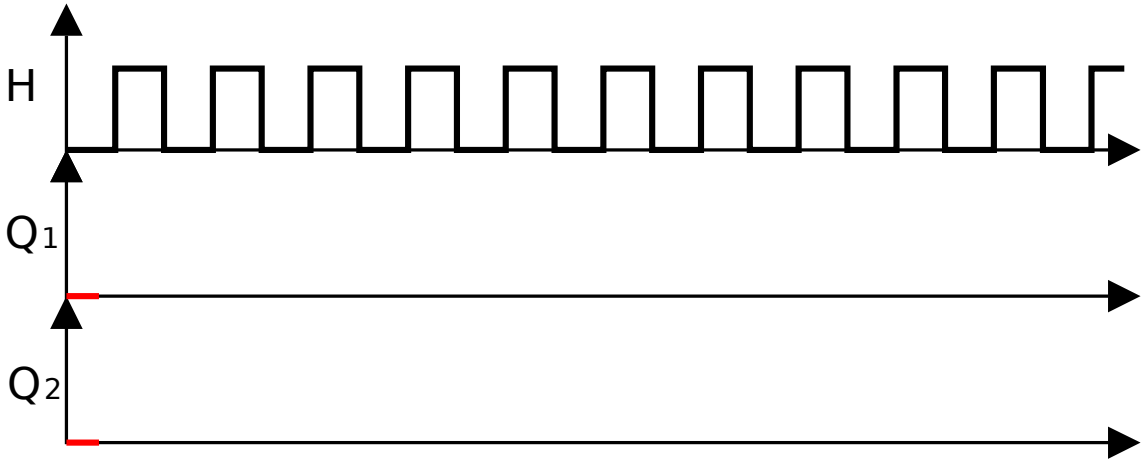


La fréquence du signal $F_q = F_H/2$



La bascule D – exercice 2





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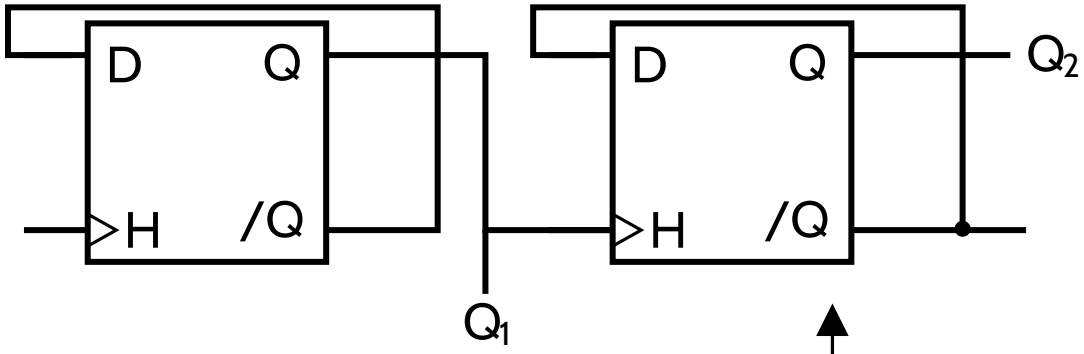
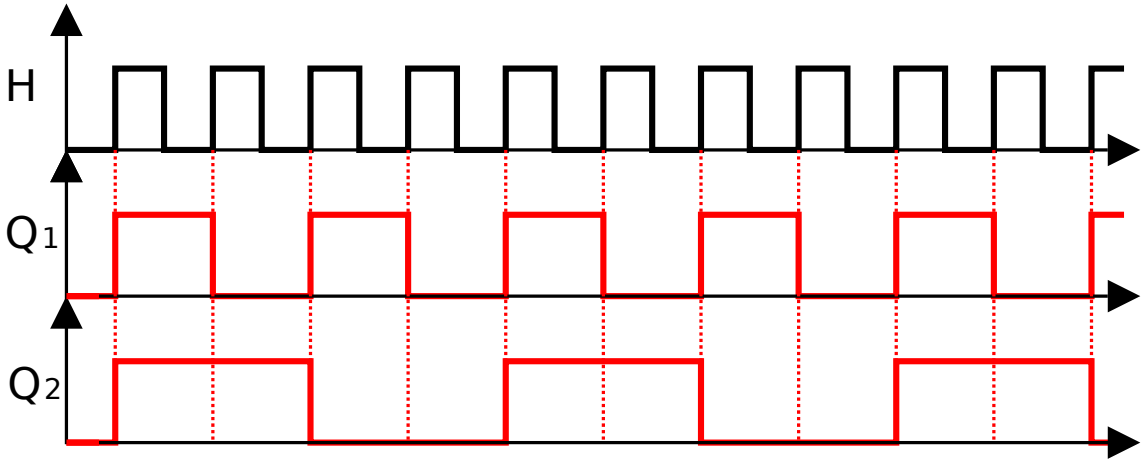
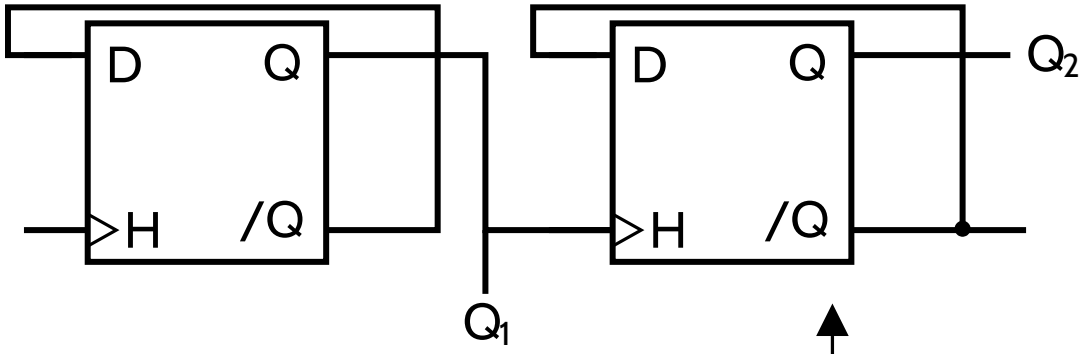
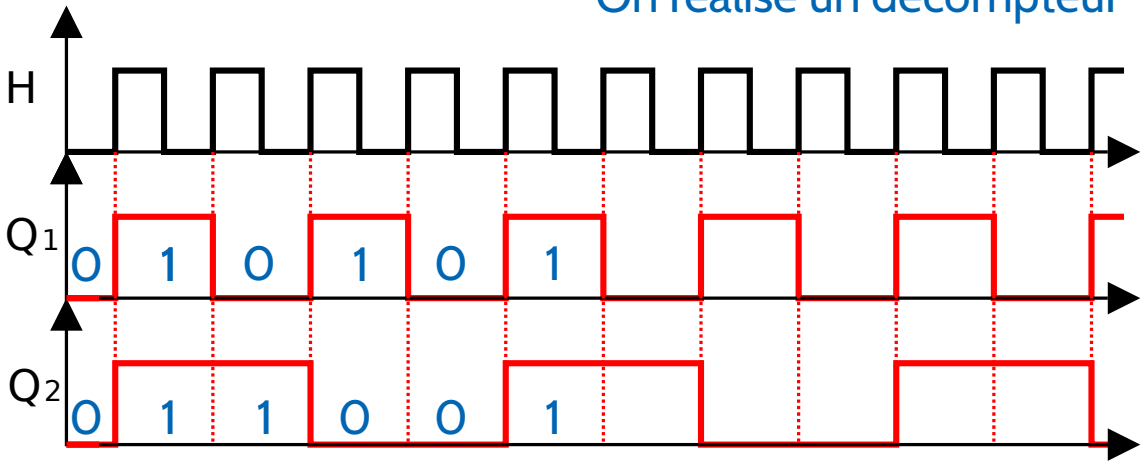




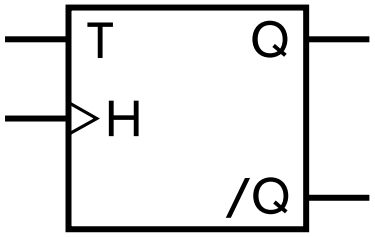
La bascule D – exercice 2



On réalise un décompteur

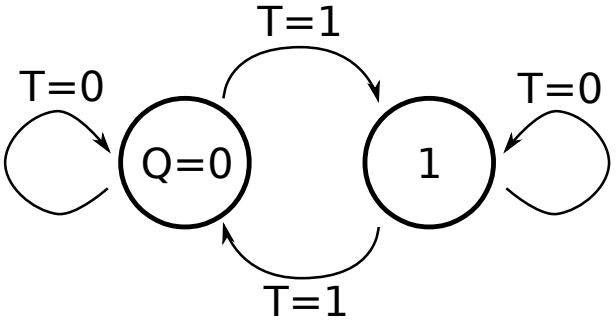


La bascule T

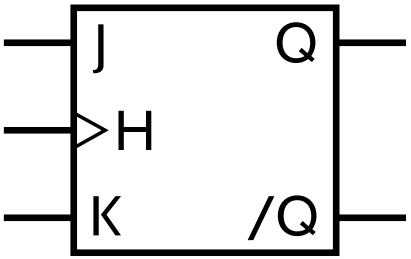


H	T	Q_{n+1}
0/1	0/1	Q_n
↑	0	Q_n
↑	1	$/Q_n$

Diagramme des états de la bascule T

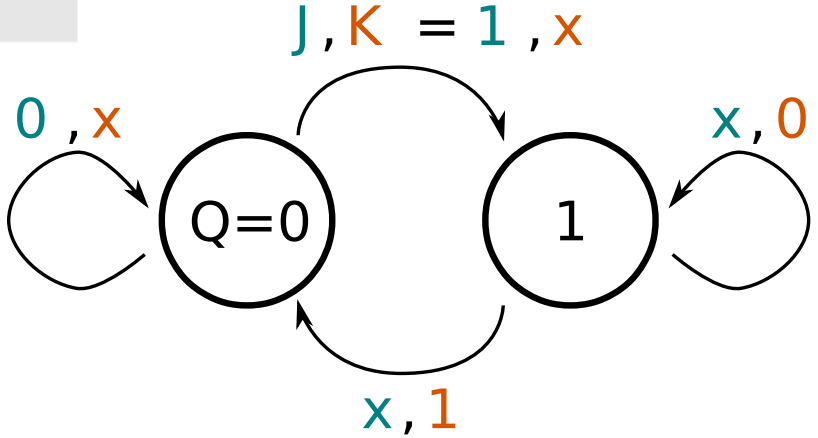


La bascule JK

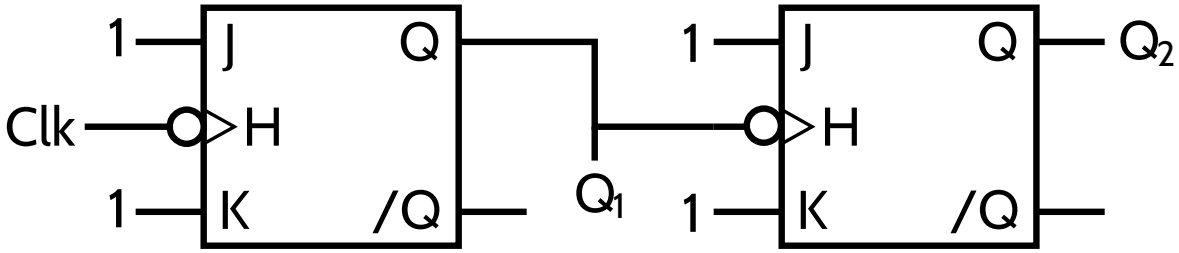


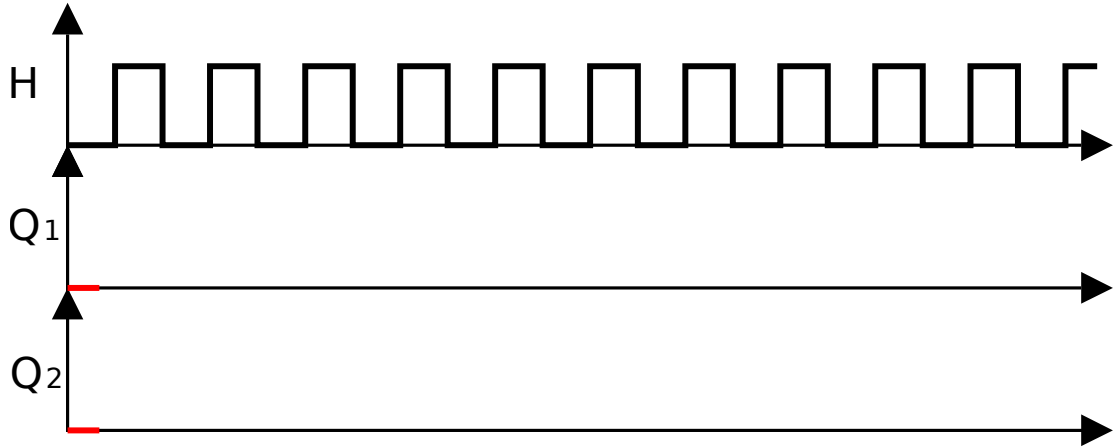
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$/Q_n$

Diagramme des états de la bascule JK

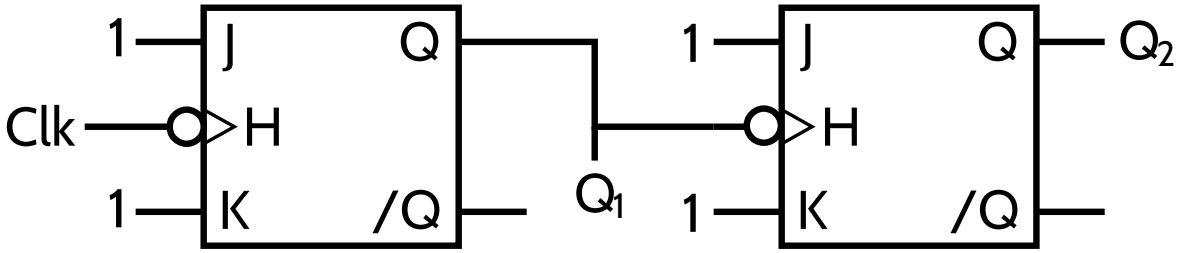


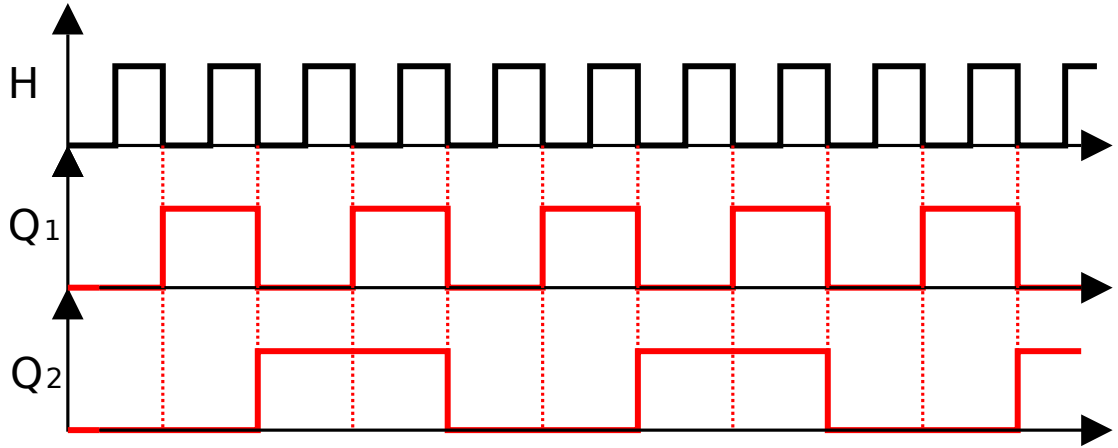
La bascule JK : exercices



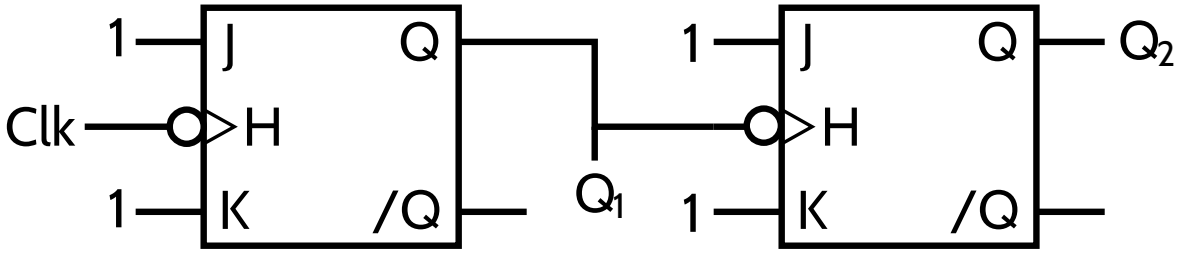


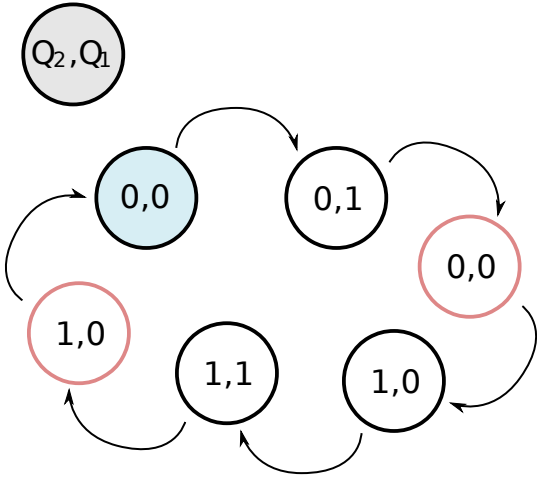
La bascule JK : exercices

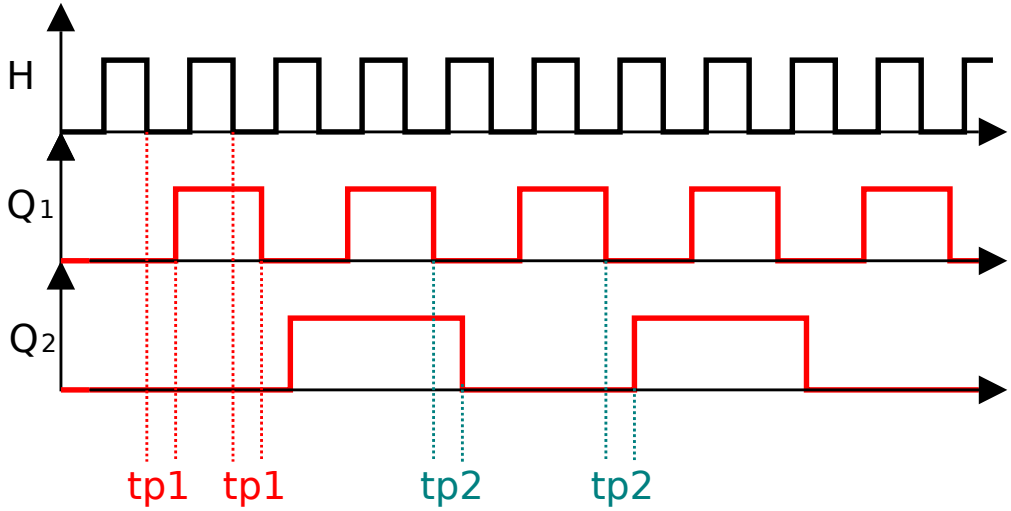




La bascule JK : exercices

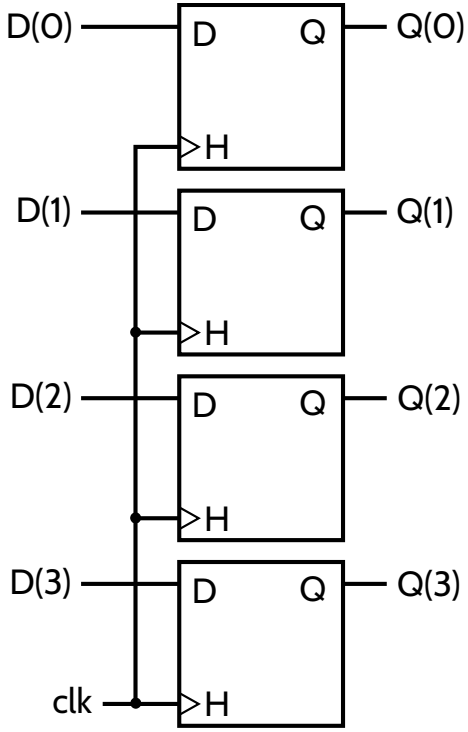


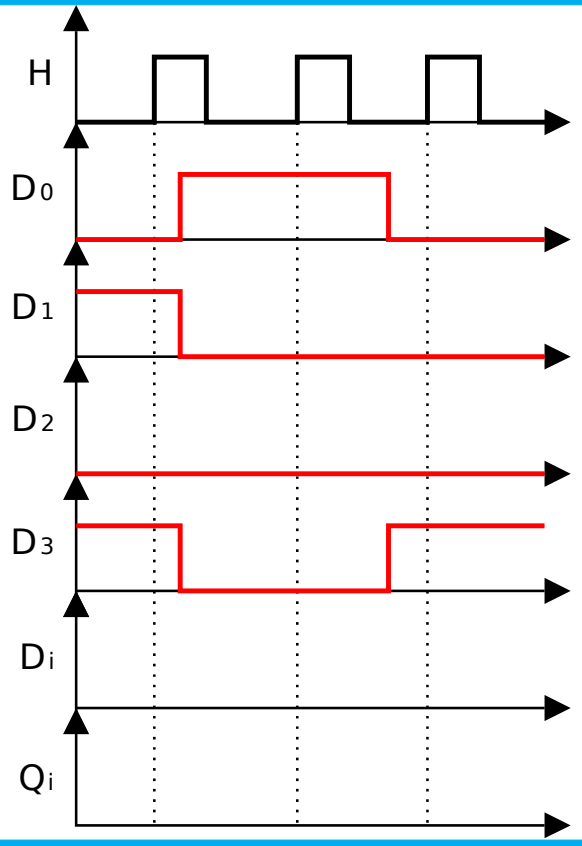




Exemples d'utilisation des bascules

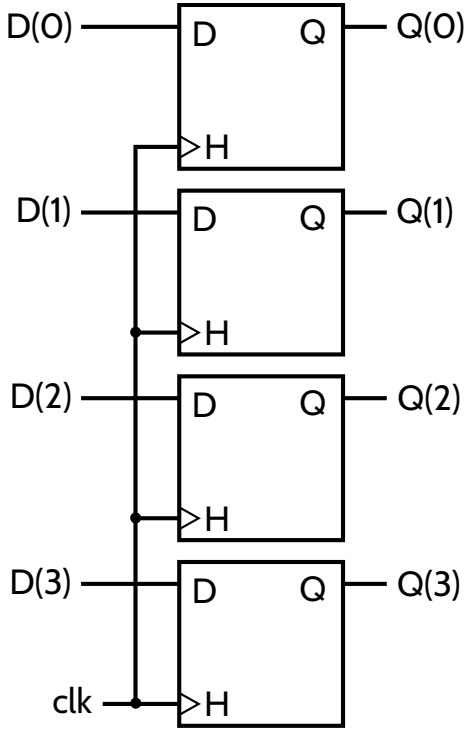
- Registre mémoire

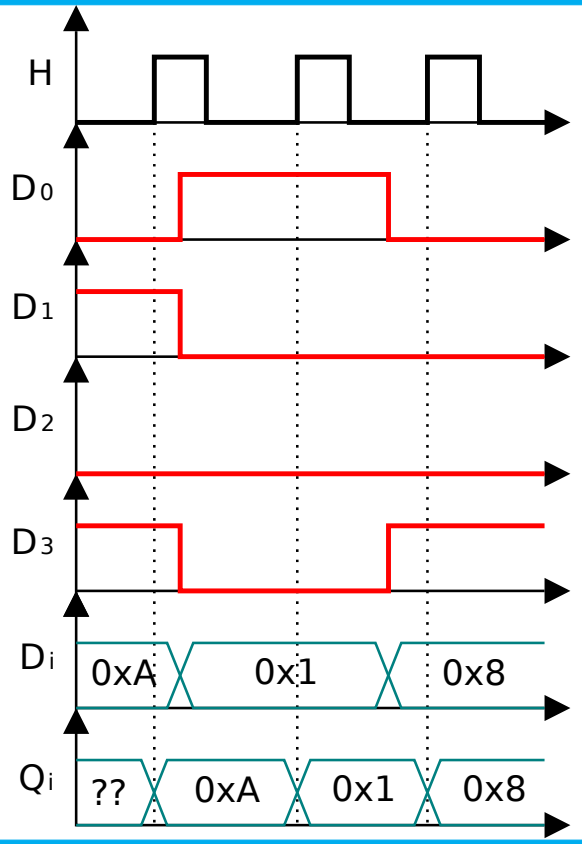




Exemples d'utilisation des bascules

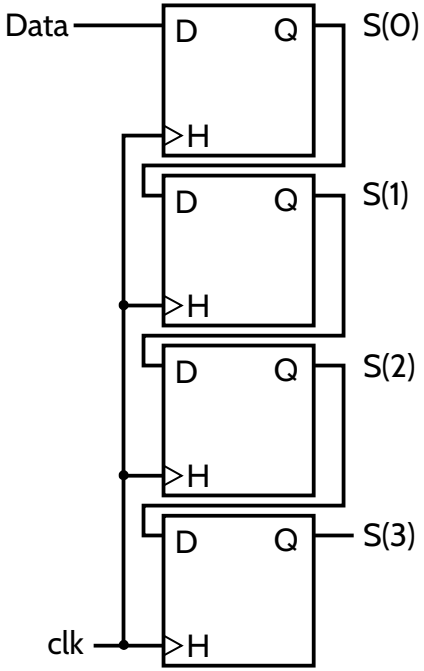
- Registre mémoire

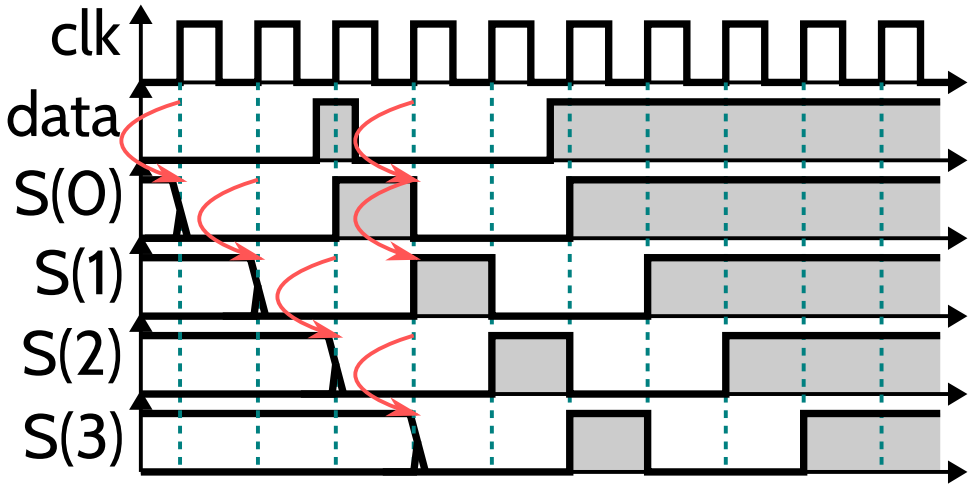




Exemples d'utilisation des bascules

- Registre à décalage

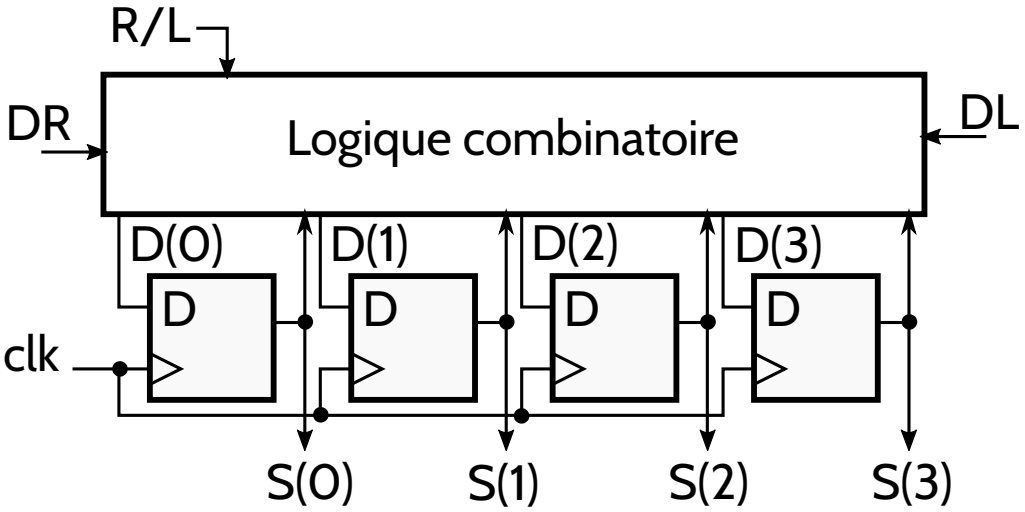




Data	S(0)	S(1)	S(2)	S(3)
0	x	x	x	x
0	0	x	x	x
0	0	0	x	x
1	0	0	0	x
0	1	0	0	0
0	0	1	0	0
1	0	0	1	0
1	1	0	0	1
1	1	1	0	0
1	1	1	1	0

Exemples d'utilisation des bascules

- Registre à décalage
  - Certains registres permettent le décalage vers la gauche ou vers la droite



$D(0) = R/L \cdot DR + \overline{R/L} \cdot S(1)$

$D(1) = R/L \cdot S(0) + \overline{R/L} \cdot S(2)$

...

$D(3) = R/L \cdot S(2) + \overline{R/L} \cdot DL$