POLYTECH ANGERS

Électronique Numérique

Les compteurs

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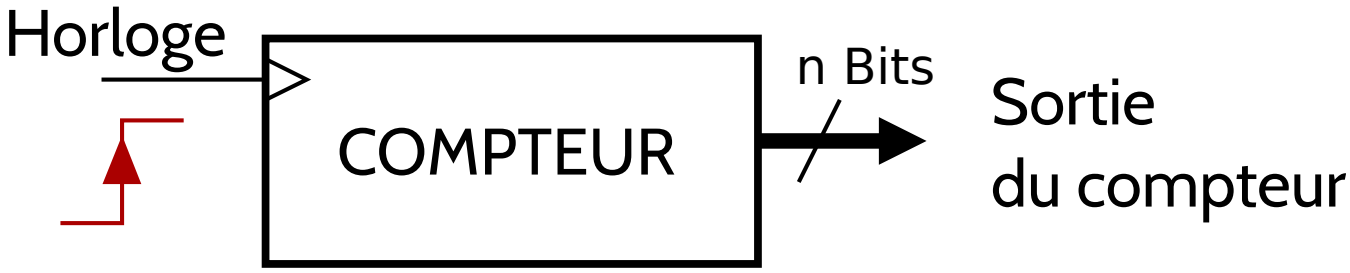
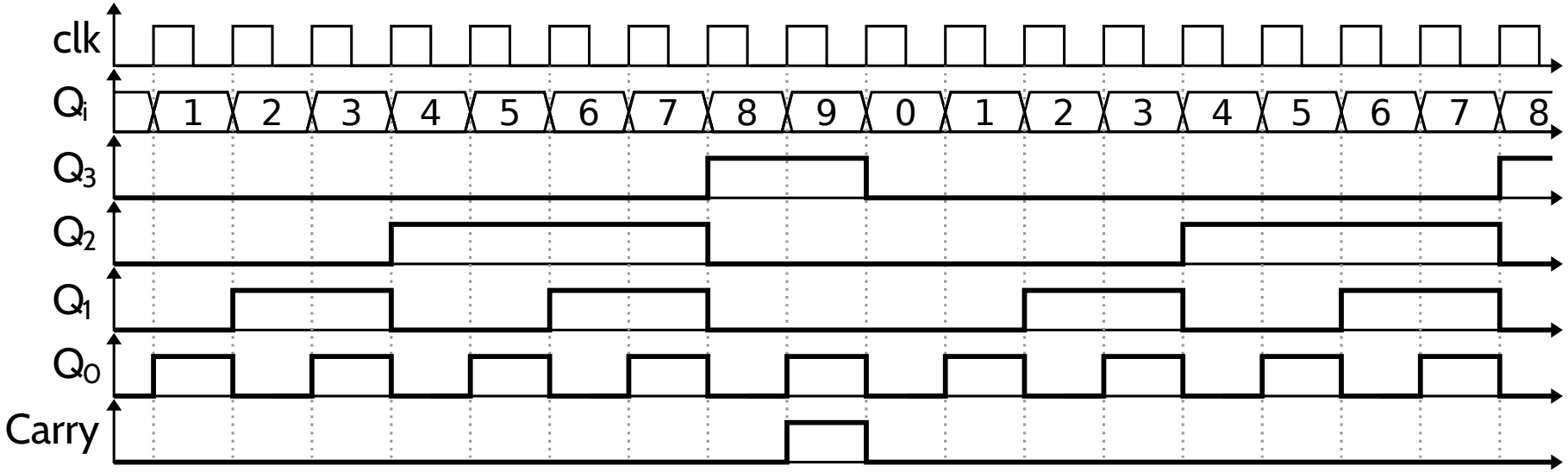
Sylvain Pezeril

Présentation



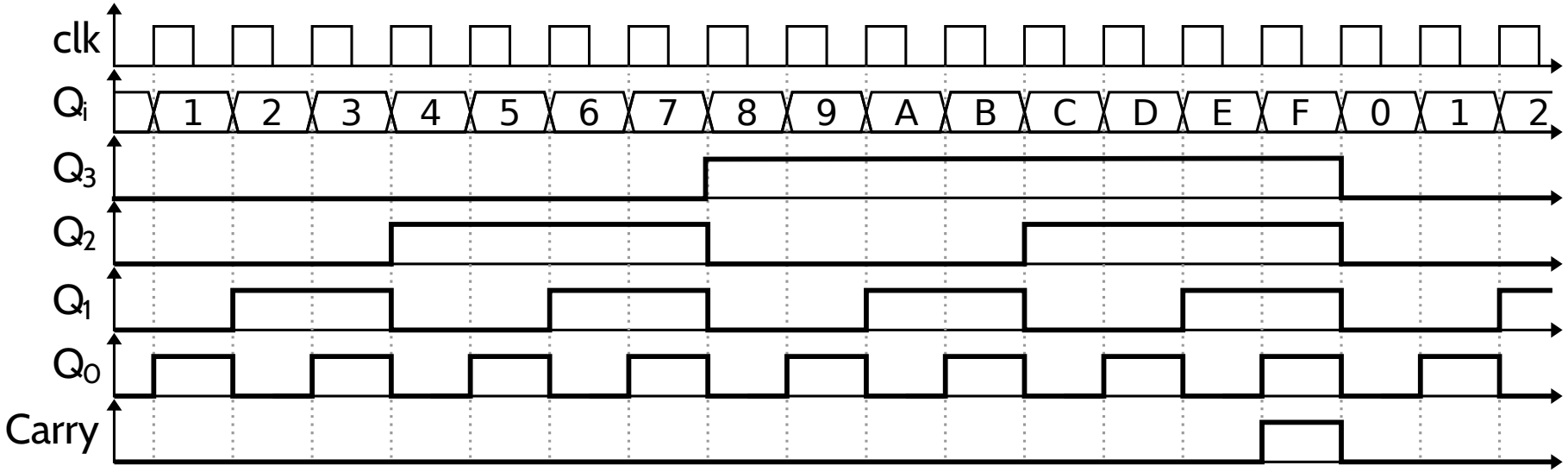
Exemples

- Compteur décimal



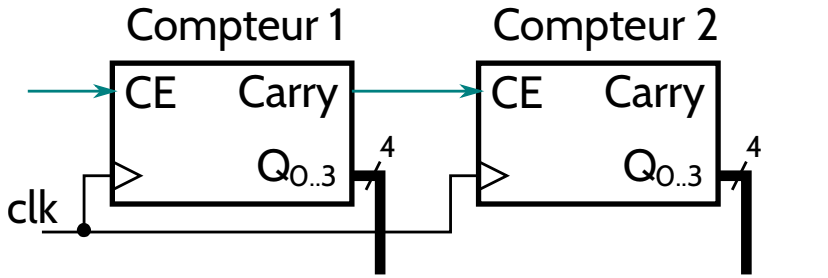
Exemples

- Compteur binaire

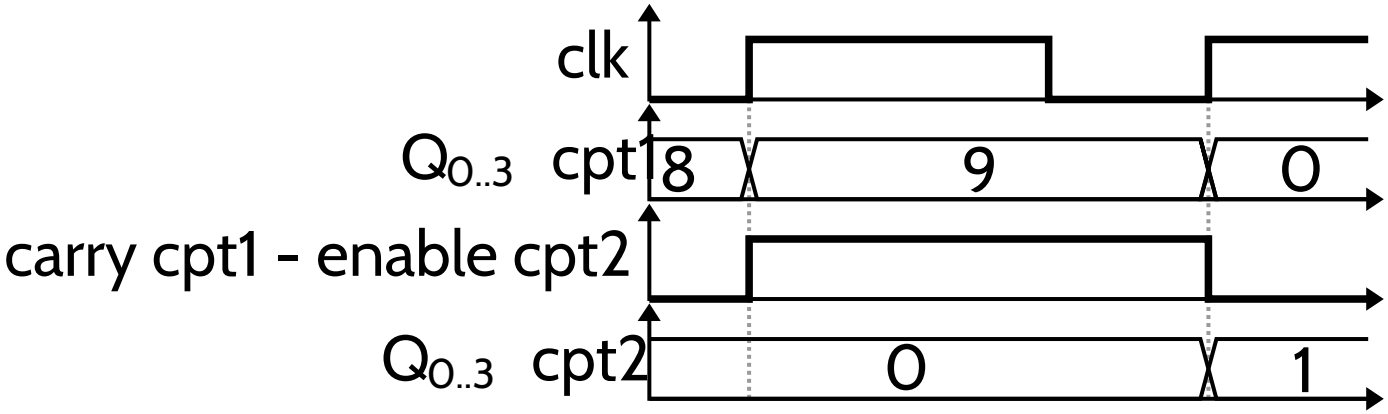


Autres fonctionnalités possibles

- Entrée de validation (Count Enable)
- Sortie de retenue (Carry)



Sorties d'un compteut 8 bits

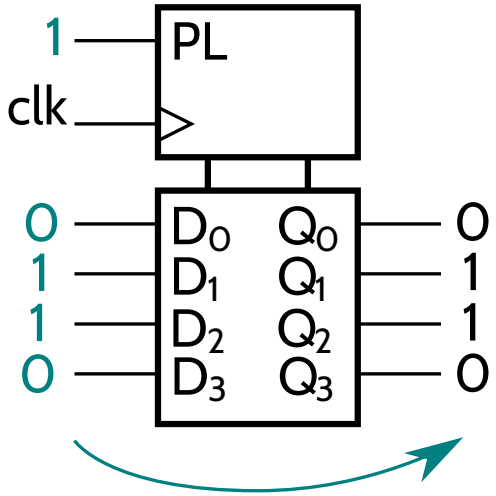


Autres fonctionnalités possibles

- Remise à zéro
  - Force toutes les sorties à 0
  - Peut être synchrone où asynchrone
    - Synchrone : Agît à un front d'horloge
    - Asynchrone : Agît directement

Autres fonctionnalités possibles

- Chargement parallèle (PL : Parallel Load)
  - Cette entrée autorise la modification des sorties prioritairement sans respecter le comptage en cours. Les sorties prennent alors la valeur des entrées de chargement parallèle



Exemple le 74HC161

74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset

Rev. 4 — 4 October 2018 Product data sheet

1. General description

The 74HC161 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW regardless of the levels at input pins CP, $\overline{PE}$, CET and CEP (thus providing an asynchronous clear function). The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}(\text{CPtoTC}) + t_{SU}(\text{CEPtoCP})}$$

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard no. 7A
- CMOS input levels
- Synchronous counting and loading

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Exemple le 74HC161

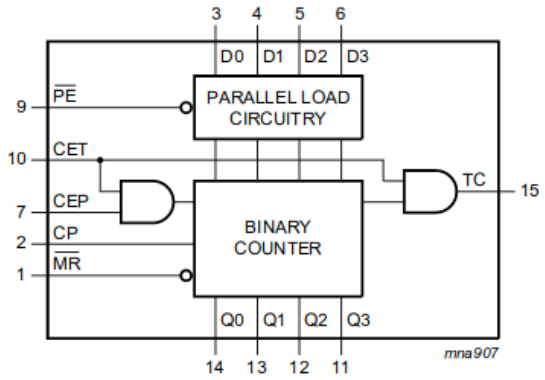


Fig. 3. Functional diagram

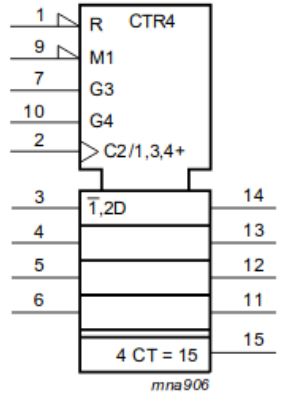


Fig. 2. IEC logic symbol

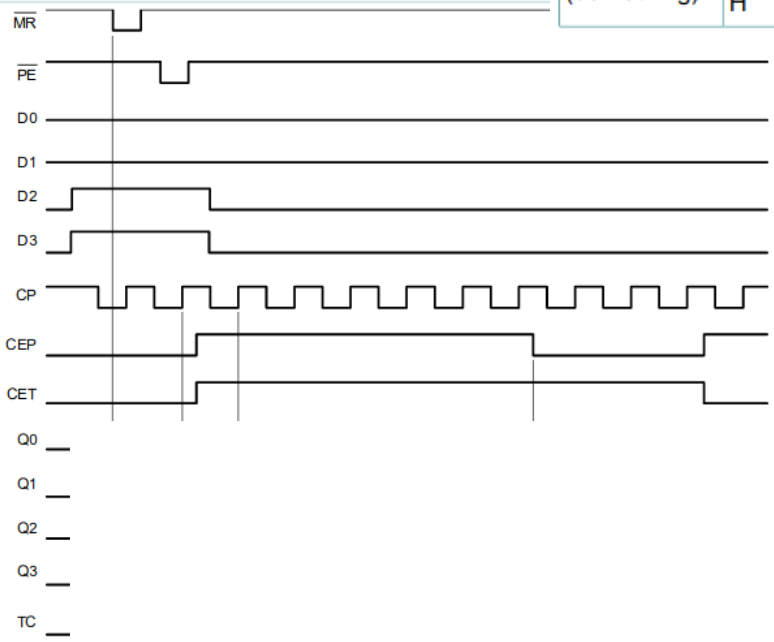
Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
$\overline{PE}$	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V_{CC}	16	supply voltage

Exemple le 74HC161

Table 3. Function table[1]

Operating modes	Input						Output	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[2]
Count	H	↑	h	h	h	X	count	[2]
Hold (do nothing)	H	X	l	X	h	X	q_n	[2]
	H	X	X	l	h	X	q_n	L



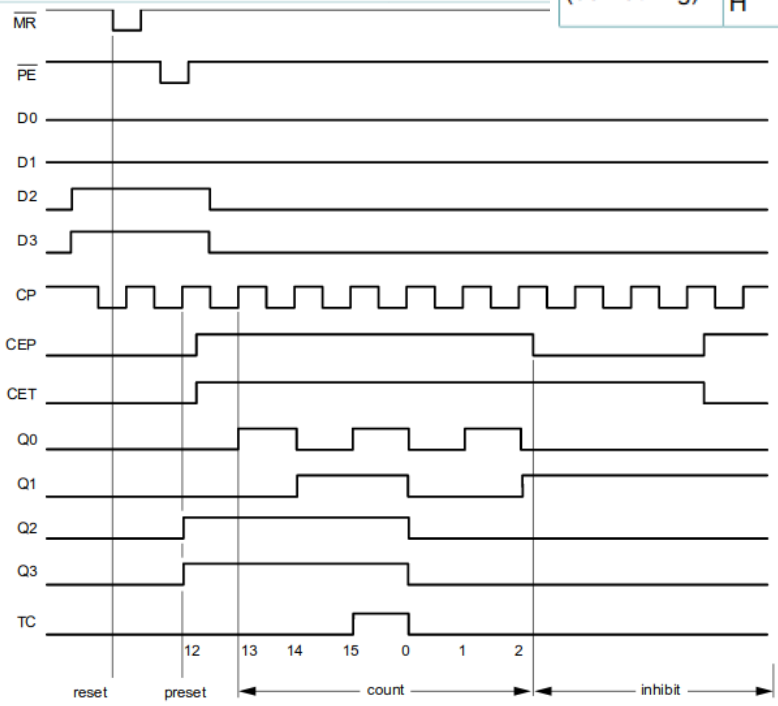
Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 8. Typical timing sequence

Exemple le 74HC161

Table 3. Function table[1]

Operating modes	Input						Output	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[2]
Count	H	↑	h	h	h	X	count	[2]
Hold (do nothing)	H	X	l	X	h	X	q_n	[2]
	H	X	X	l	h	X	q_n	L



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 8. Typical timing sequence

Exemple : le 74HC161

- Caractéristiques
  - Compteur binaire 4 bits (0 – 15)
  - Chargement parallèle synchrone, actif à 0
  - Reset asynchrone actif à 0
  - 2 entrées de validation (la différence se fait sur la gestion de la retenue)

Constitution d'un compteur

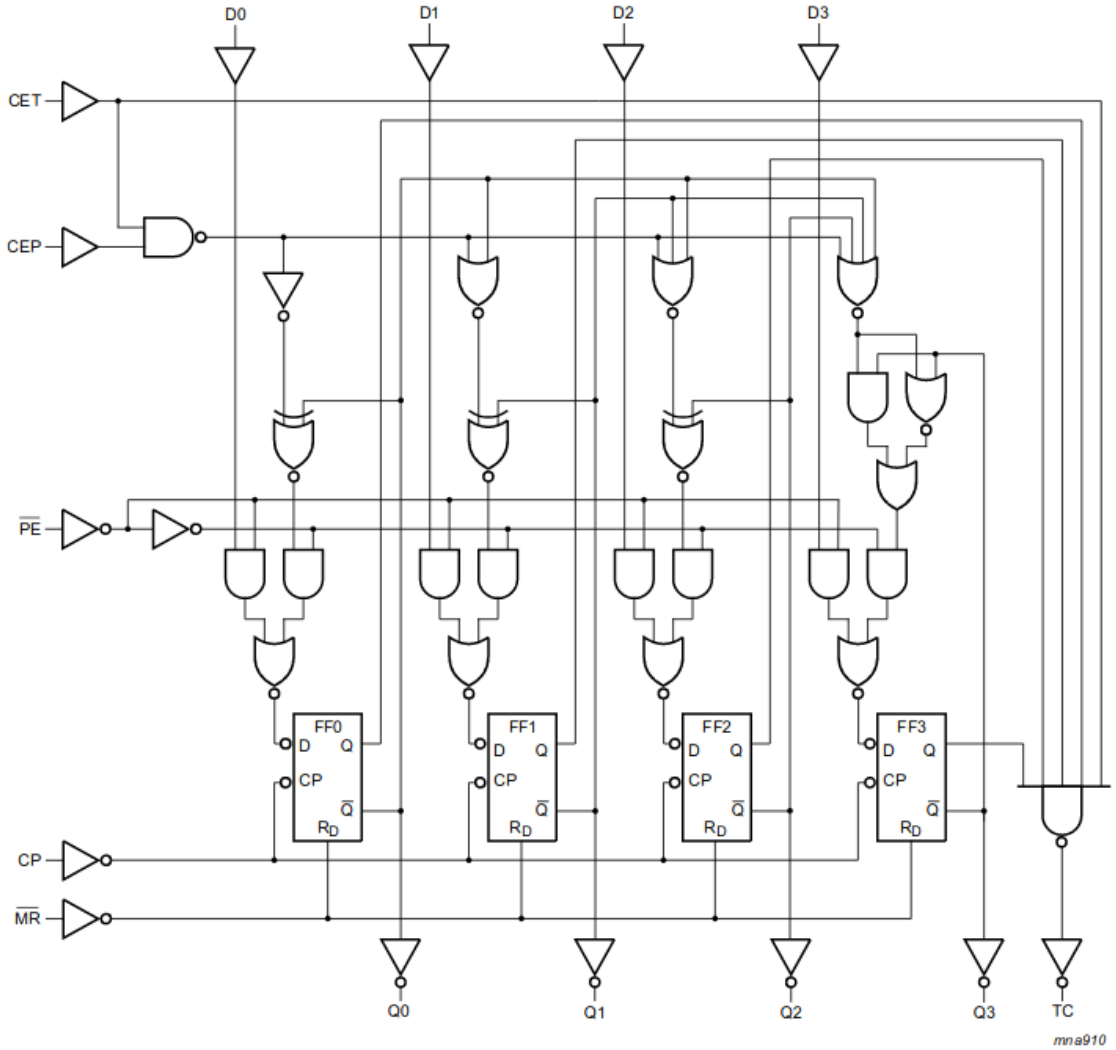


Fig. 4. Logic diagram

Constitution d'un compteur

Logique combinatoire

Logique séquentielle

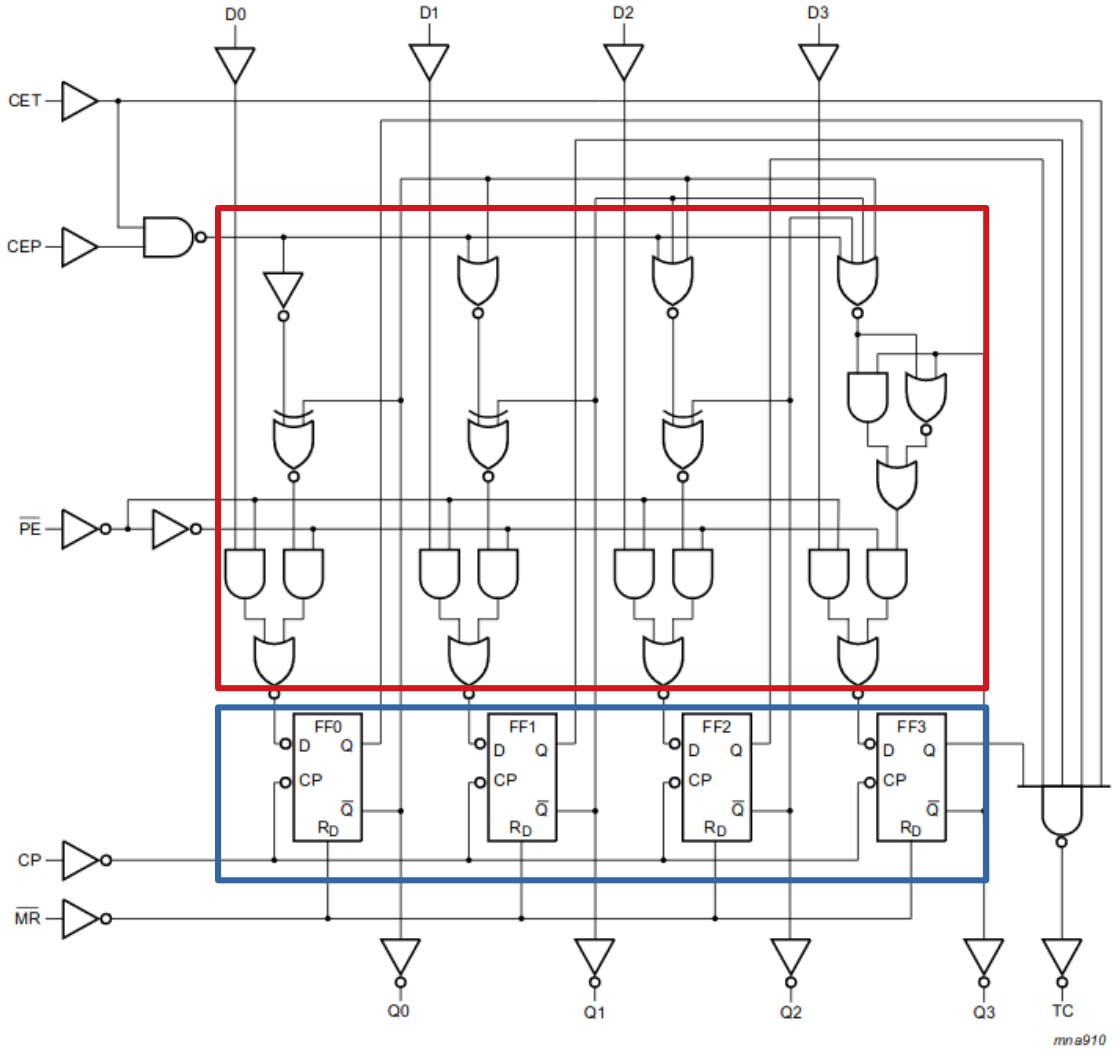
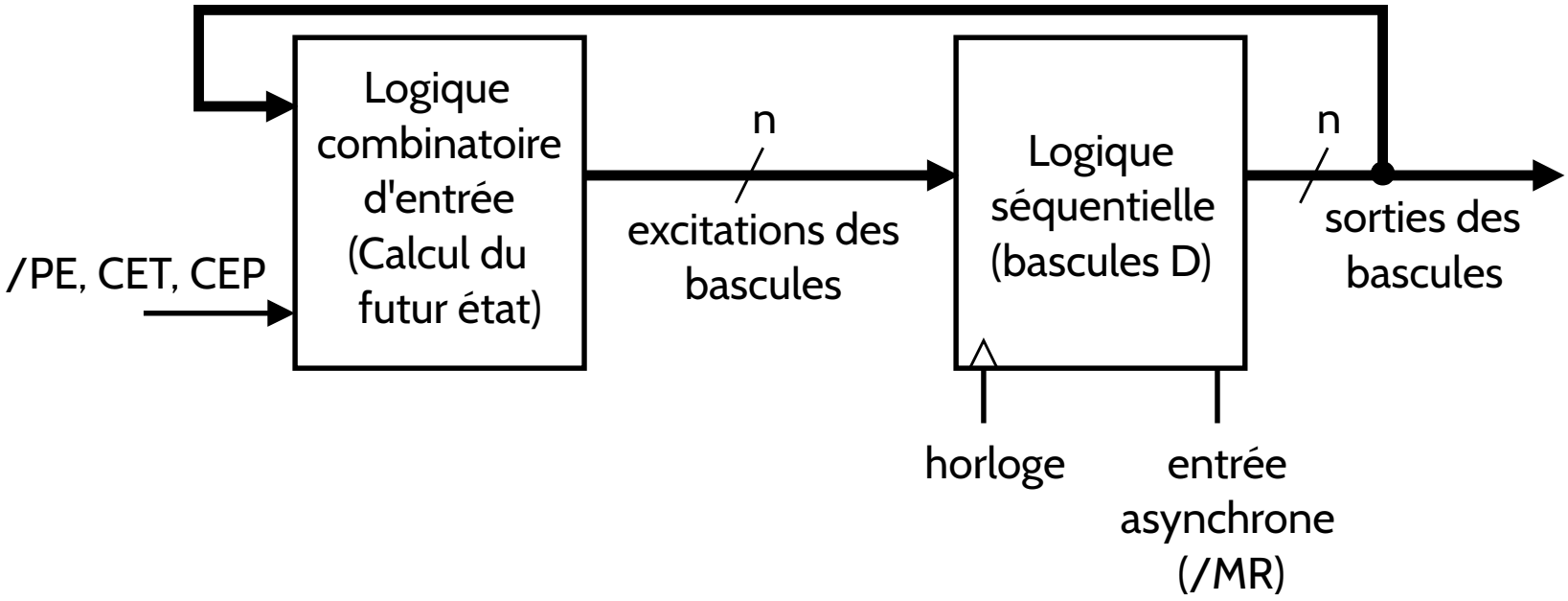
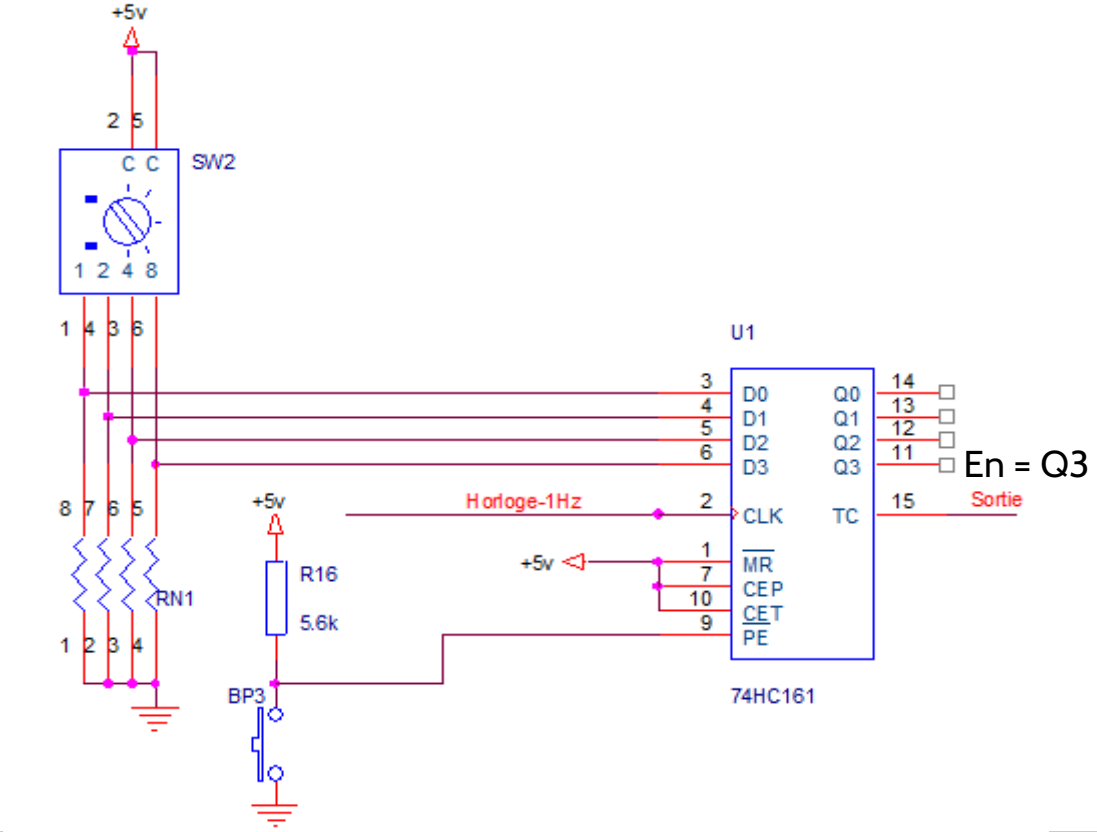


Fig. 4. Logic diagram

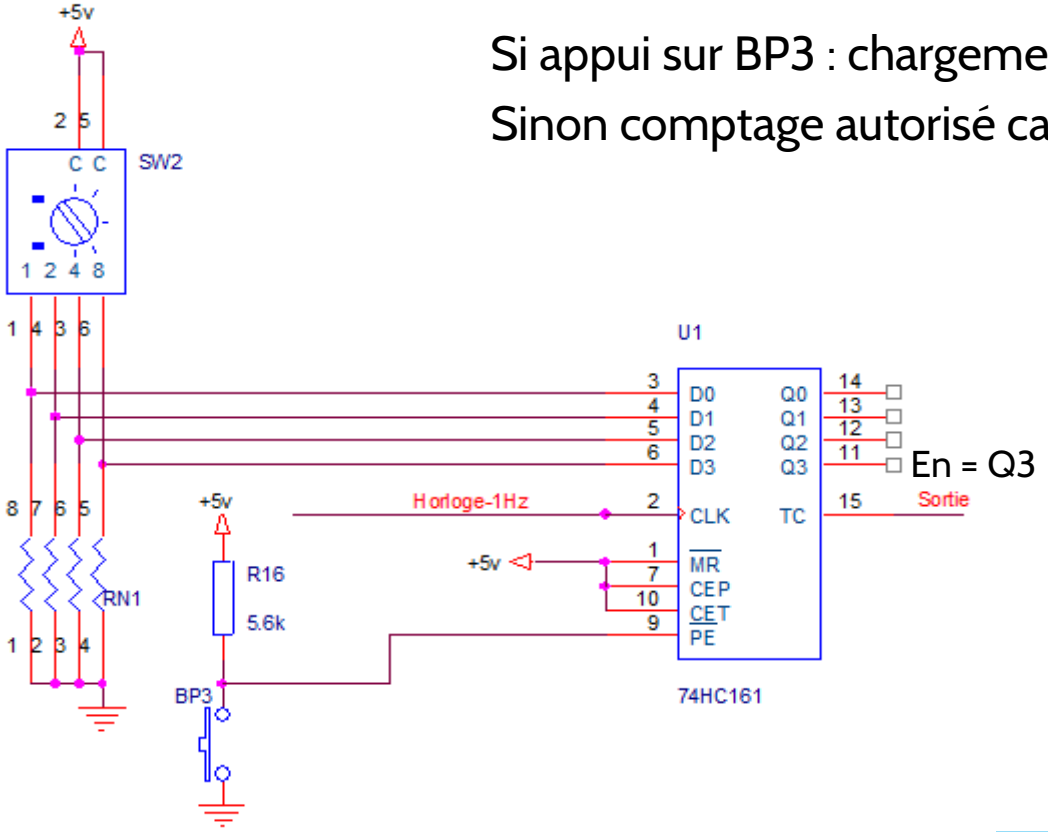
Constitution d'un compteur



Utilisation des compteurs



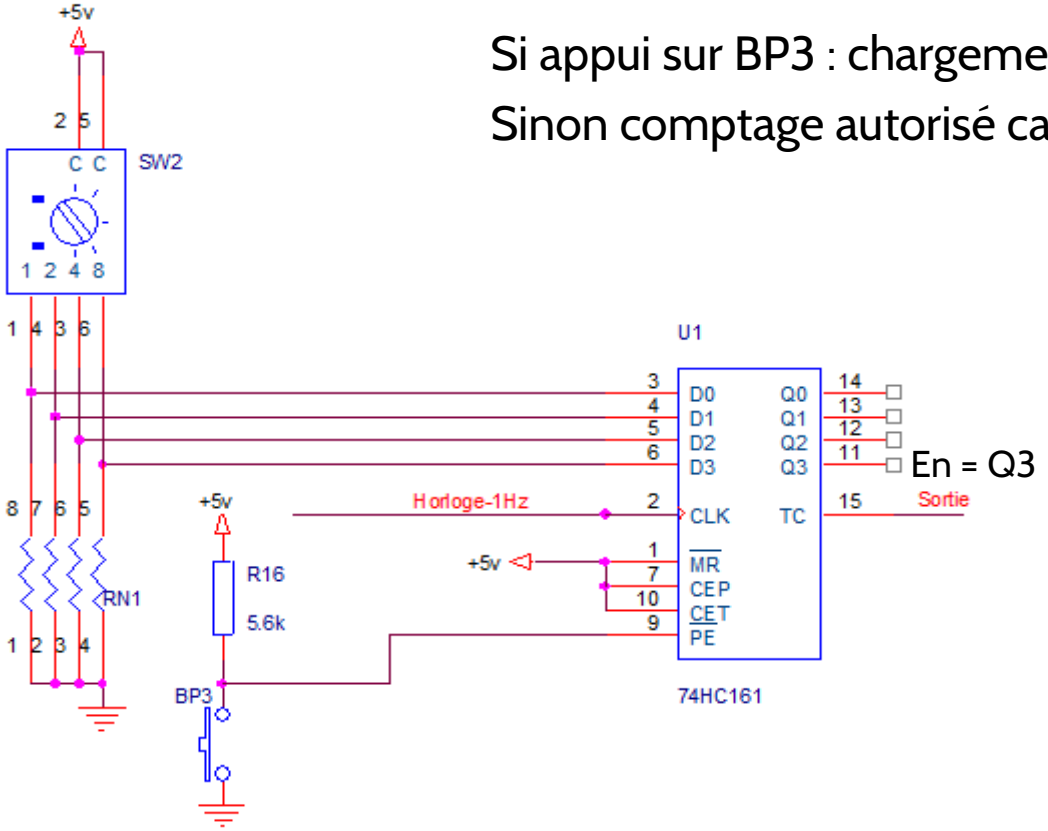
Utilisation des compteurs



Si appui sur BP3 : chargement parallèle en Q_i selon roue codeuse

Sinon comptage autorisé car CEP = CET = 1

Utilisation des compteurs



Si appui sur BP3 : chargement parallèle en Q_i selon roue codeuse

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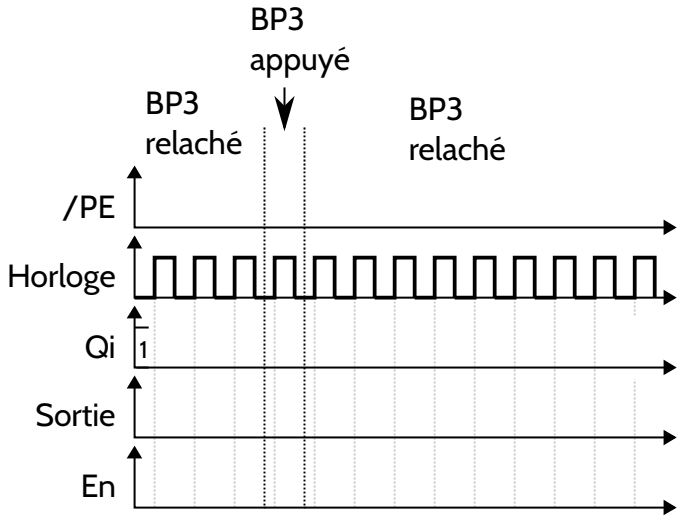
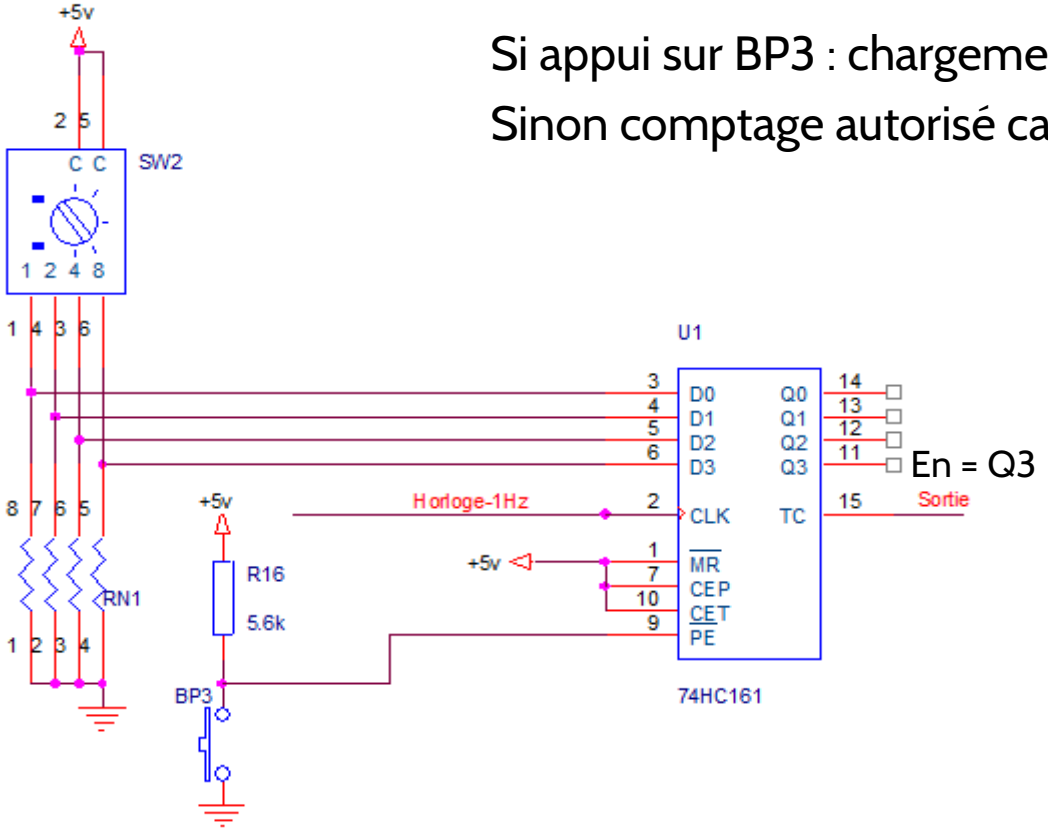
Hypothèse : roue codeuse = 7



Utilisation des compteurs



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